RESEARCH ARTICLE | MARCH 21 2025

A nano-scale design of Vedic multiplier for electrocardiogram signal processing based on a quantum technology

Yuyao Wang; Mehdi Darbandi ; Seyed-Sajad Ahmadpour ; Nima Jafari Navimipour ;
Ahmad Habibizad Navin; Arash Heidari ; Mehdi Hosseinzadeh ; Mohammad Anbar

APL Mater. 13, 031114 (2025)
https://doi.org/10.1063/5.0241549

A nano-scale design of Vedic multiplier for electrocardiogram signal processing based on a quantum technology

Cite as: APL Mater. 13, 031114 (2025); doi: 10.1063/5.0241549
Submitted: 30 September 2024 • Accepted: 6 February 2025 •
Published Online: 21 March 2025

Yuyao Wang,[1] Mehdi Darbandi,[2,a)] Seyed-Sajad Ahmadpour,[3,b)] Nima Jafari Navimipour,[3,4,5,c)] Ahmad Habibizad Navin,[6] Arash Heidari,[7,d)] Mehdi Hosseinzadeh,[8,9,c)] and Mohammad Anbar[10]

AFFILIATIONS

[1]McCoy School of Engineering, Midwestern State University, Wichita Falls, Texas 76308, USA
[2]Pôle Universitaire Léonard de Vinci, Paris, France
[3]Department of Computer Engineering, Faculty of Engineering and Natural Sciences, Kadir Has University, Istanbul, Turkey
[4]Future Technology Research Center, National Yunlin University of Science and Technology, Douliou, Yunlin, Taiwan
[5]Research Center of High Technologies and Innovative Engineering, Western Caspian University, Baku, Azerbaijan
[6]Department of Computer Engineering, Tabriz Branch, Islamic Azad University, Tabriz 5157944533, Iran
[7]Department of Computer Engineering, Faculty of Engineering and Natural Science, İstanbul Atlas University, Istanbul, Türkiye
[8]School of Computer Science, Duy Tan University, Da Nang, Vietnam
[9]Jadara Research Center, Jadara University, Irbid 21110, Jordan
[10]Communication Technology Engineering Department, Tartous University, Tartus, Syria

[a)]**Email:** mehdi.darbandi@edu.devinci.fr
[b)]**Email:** s.ahmad@khas.edu.tr
[c)]**Authors to whom correspondence should be addressed:** nima.navimipour@khas.edu.tr; JNNima@yuntech.edu.tw; and mehdihosseinzadeh@duytan.edu.vn
[d)]**Email:** arash.heidari@atlas.edu.tr

ABSTRACT

An electrocardiogram (ECG) measures the electric signals from the heartbeat to diagnose various heart issues; nevertheless, it is susceptible to noise. ECG signal noise must be removed because it significantly affects ECG signal characteristics. In addition, speed and occupied area play a fundamental role in ECG structures. The Vedic multiplier is an essential part of signal processing and is necessary for various applications, such as ECG, clusters, and finite impulse response filter architectures. All ECGs have a Vedic multiplier circuit unit that is necessary for signal processing. The Vedic multiplier circuit always performs multiplication and accumulation steps to execute continuous and complex operations in signal processing programs. Conversely, in the Vedic multiplier framework, the circuit speed and occupied area are the main limitations. Fixing these significant defects can drastically improve the performance of this crucial circuit. The use of quantum technologies is one of the most popular solutions to overcome all previous shortcomings, such as the high occupied area and speed. In other words, a unique quantum technology like quantum dot cellular automata (QCA) can easily overcome all previous shortcomings. Thus, based on quantum technology, this paper proposes a multiplier for ECG using carry skip adder, half-adder, and XOR circuits. All suggested frameworks utilized a single-layer design without rotated cells to increase their operability in complex architectures. All designs have been proposed with a coplanar configuration in view, having an impact on the circuits' durability and stability. All proposed architectures have been designed and validated with the tool QCADesigner 2.0.3. All designed circuits showed a simple structure with minimum quantum cells, minimum area, and minimum delay with respect to state-of-the-art structures.

I. INTRODUCTION

Biomedical digital signal processing is widely utilized in medicine to diagnose various body parts. An electrocardiogram (ECG) signal analysis can be used to learn more about pathology and cardiac health.[1,2] Continuous remote cardiac monitoring can improve patient autonomy and care quality while improving older patients' mobility.[3] The ECG signal creates a composite image of the mechanical and electrical performance of the heart throughout time from different perspectives or projections.[4] Several electrodes are positioned on various body parts to capture the ECG signal. Each slight electrical change on the skin that happens by heartbeat or depolarization is detected and amplified in an ECG to produce an ECG signal.[5] An essential component in processing an ECG signal for a healthy heartbeat is a Vedic multiplier circuit, a sophisticated math device developed through age-old mathematics in India.[6,7] It is a key component in accurately amplifying and processing complex electrical impulses generated through a heartbeat. Creation and installation of a Vedic multiplier circuit is essential in an ECG signal path, and any flaw in its configuration can generate significant difficulty.[6,7]

The absence of a Vedic multiplier with a proper configuration can affect key factors, resulting in high noise, an increased chip footprint, and inefficient execution performance.[8] All such factors not only have a technical basis but also have important implications for ECG reading quality and reliability, and they rely on them.[9] High noise can overshadow sensitive but critical information regarding heart electrical activity, an increased footprint can result in a high production cost and reduced efficiency in chip development, and an inefficient execution can make real-time processing capabilities essential for timely diagnosis and observation sluggish. These inherent faults in the circuit configuration have a detrimental impact on extracting critical information from ECG waves and, in extreme cases, can result in incorrect interpretations of heart state.[9] Incorrect interpretations can have disastrous consequences, and in medical environments, correct readings are paramount for the proper care of a patient. Therefore, one of biomedical engineering's biggest challenges is developing an ECG filter with the best of a Vedic multiplier circuit.[10] What is desired is a robust system with high accuracy in selecting faint ECG signals in any environment with a mix of interfering noises, and yet with traditional Complementary Metal–Oxide–Semiconductor (CMOS) technology. What is at issue is resolving the inbuilt contradictions between noise suppression, chip area, and processing speed, with a view toward delivering added dependability and accuracy in ECG diagnostics.

Fixing these vital flaws can severely affect the performance of this critical circuit. The use of quantum computing technologies[11] is one of the most popular solutions to overcome all previous shortcomings, such as the high occupied area, lack of stability, and lack of high speed. In other words, a high-performance quantum technology like quantum dot cellular automata (QCA)[12] operates based on clusters of quantum dots and can resolve all prior shortcomings. In this paper, an effective Vedic multiplier is being proposed for ECG devices using the CSA, half-adder, and XOR gate employing the QCA technology. In the proposed structures, a single-layer design without cell rotation has been implemented. The QCADesigner 2.0.3 tool is employed to develop and verify the proposed architecture. The designed circuits have basic frameworks with a minimum number of quantum cells and an optimal area with a low delay. The essential contributions of this article are as follows:

- Introducing a new half-adder architecture based on normal cells that reduces area and clock cycles with computational efficiency, utilizing inherent parallelism in QCA clusters.
- Presenting a single-layer CSA design for QCA clusters parallel processing based on simple quantum cells, considering the low-occupied area and clock cycle.
- Executing a Vedic multiplier structure utilizing the XOR, half-adder, and CSA structures for ECG signals, capitalizing on the inherent advantages of QCA clusters in optimizing the computational process.

Section II presents a detailed analysis of QCA technology: cells, basic gates, wires, and clocks. Section III presents related work in the form of a literature review concerning multiplier circuits in ECG applications. Section IV presents some proposed designs. Section V compares and discusses the results of the simulations. Finally, Sec. VI presents the conclusions based on the work presented.

II. INTRODUCTION TO QCA TECHNOLOGY

The most critical component in QCA technology is the quantum cell.[13] In a quantum cell, four dots line the four corners of a square. Through Coulombic collaboration, it is possible to calculate the presence of extra electrons in quantum dots. All quantum dots on the cell's surface are square and measure just a few nanometers in size.[14] Two of the electrons in each cell can be used to create a quantum tunnel between two points. Because of electron repulsion, the dots in these are oriented counterclockwise from corner to corner.[15] Having two electrons means that cells can store twice as much information (additionally named cell polarization P).[16,17] There are two distinct polarizations: P = 1 for the "0" and "1" double states and P = +1 for the "1" double state. Figure 1 shows the 90° and 45° QCA cells, each with a paired conduct.

QCA circuits comprise the following fundamental elements: an inverter, wires, and a three-input majority gate. In order to generate double respect from one side to the next, depending on Coulomb connections, a 90° QCA wire is constructed by descending QCA cells, as demonstrated in Fig. 2(a). Each cell in a 45° QCA cable has the opposite polarization as its neighboring cell, which depicts a coplanar wired crossing, which is achieved by employing two types of wires in a mirror-image configuration.[18] A majority gate and an inverter are illustrated in Fig. 2(b) as the primary QCA inputs. The QCA inverter's implementation is shown in Fig. 2(c). After being

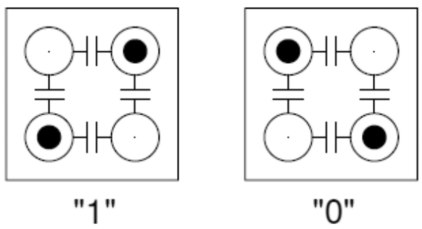

FIG. 1. Two charge arrangements in a QCA cell.

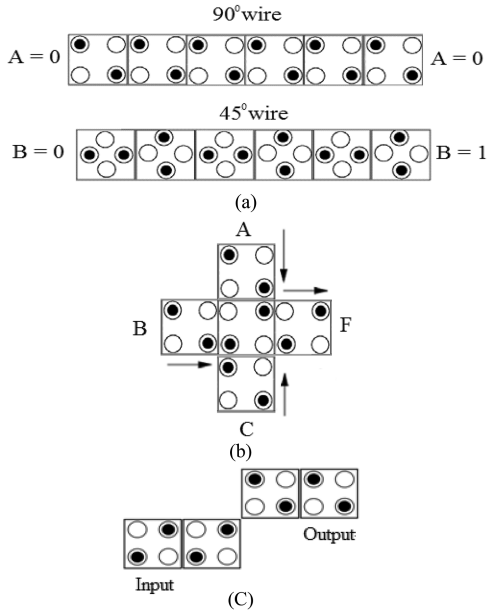

FIG. 2. (a) QCA wires, (b) QCA architecture related to the 3-input majority gate, and (c) QCA-based design associated with the inverter gate.

split between two QCA wires, the supplementary information is displayed at the fusion node.

It is important to synchronize the data-coordinating information needed to produce increasingly complicated QCA frameworks (as such estimation). To ensure that QCA circuits run smoothly, this task is completed by the QCA clock.[19] Time-based sample collections using the clock are possible (clock zones). Multiple QCA cells are activated within each clock zone, with their output feeding into the succeeding zone as per the clock design. A diagram of QCA's adiabatic timing is shown in Fig. 3. The clock signal consists of a series of four phases separated by a 90° angle: hold, switch, relax, and release. In the switch phase, the cell becomes enamored with its surroundings when it activates Coulombic cooperation with nearby cells.[19]

III. LITERATURE REVIEW

Mohanty and Patel[20] proposed the new processes that were required to enhance the conventional carry select adder (CSLA).

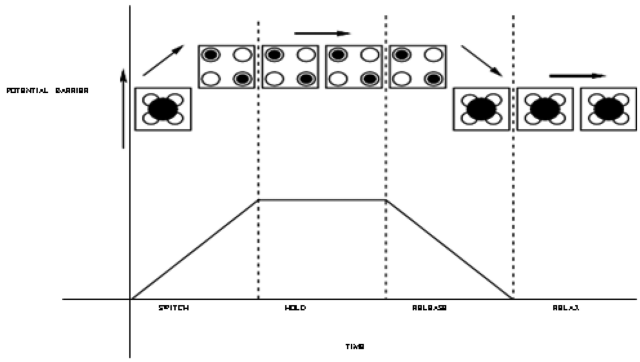

FIG. 3. Types of clocking in QCA.

They examined CSLA in accordance with binary to excess-1 converter (BEC) to recognize data dependence and redundant logic operations. To enhance conventional CSLA, new logic operations were implied, eliminating all redundant logic operations. Before evaluating the final sum, the proposed schedule carry select (CS) scheme differs from conventional techniques. For optimization of the CS logic and generation unit, two envisioned patterns of carry word's bit and fixed *cin* bits are used. For acquiring efficient CSLA, optimized logic units were designed. Compared with BEC-based CSLA, this proposed CSLA involved less delay and area. Because of the small-carry-output delay, it can be used for square-root (SQRT) CSLA.

Verma and Sampath Kumar[21] designed and analyzed a carry look-ahead adder (CLA) using a carry select adder. The CMOS process designs adders with 0.18 μm. The regular CSLA adders are developed based on the area.

Savita *et al.*[22] used the 45 nm CMOS process technology with a simple gate-level modification to reduce CSLA delay and area. CSLA was utilized in various data-processing processors to conduct high-speed arithmetic functions, and then the 180 nm CMOS technology was used to design a 16-bit CSLA. The 45 nm technology-based CSLA structure outperforms standard CSLA, designed with the 180 nm technology.

Saxena *et al.* [23] proposed modifying the conventional carry select adder to generate better performance than the conventional carry select adder with 8-bit, 16-bit, 32-bit, and 64-bit CSLA frameworks. It is also a little bit faster than all the other adders. It was also probably quicker than some other full adders. As a result of having a smaller area and low power, the suggested SQRT CSLA had a lower

TABLE I. A detailed analysis of prior CSA.

Authors	Terminology	Benefits	Drawbacks	Simulation tools
Mohanty and Patel[20]	CS	Less delay and area	High power consumption	VHDL
Verma and Sampath Kumar[21]	CLA	Multiplier-based	High area	Xilinx 9
Savita *et al.*[22]	CSLA	High speed	High power consumption (CMOS)	Not reported
Saxena *et al.*[23]	CSLA	Low area and low power	Conventional and old structure	Verilog-HDL
Shanigarapu and Shrivastava[24]	Finite impulse response	Reduced power dissipation	High complexity	Verilog-HDL

transistor count, making it simple and effective for VLSI-embedded applications.

Shanigarapu and Shrivastava[24] proposed the generation of carry, which was an essential step in the design of adders as it minimizes the number of transistors in the adder to reduce the data path power consumption. The design reduced the power, delay, and space. Instead of the RCA cascade, the proposed design employed a D-latch for Cin = 0 or Cin = 1. Hence, based on the current technique, the authors created an effective PPAVD-RCA-based Finite Impulse Response (FIR) filter for ECG devices.

Table I provides an analysis of the previously discussed CSA in terms of its methods, benefits, drawbacks, and simulation tools.

IV. SUGGESTED FRAMEWORK

This part explains ECG for Vedic multiplier-based biomedical signal processing. After that, a half-adder will be suggested, and then, the proposed CSA will be provided based on the half-adder. Finally, a Vedic multiplier is recommended, considering all possible circuits in biomedical signal processing systems.

A. Electrocardiogram for biomedical signal processing

Biomedical signal processing has become prevalent in health care to identify various illnesses in various parts of the human body.[25,26] Periodic remote cardiac and brain monitoring is utilized to increase older people's mobility and autonomy and to address health-related concerns.[27,28] An ECG signal investigation is a useful tool for learning about diseases and cardiac health because it provides an integrated picture of the physical and electrical performance of the heart from various perspectives or projections at various time intervals.[27] Electrodes have been placed on different body parts to detect ECG impulses.

The full installation to build a DSP-based ECG system is illustrated in Fig. 4, which includes several electrodes, an ECG preamplifier board, a DSP Starter Kit (DSK) with a 3.5 mm audio input, and a Pentium IV Desktop PC. The DSP-based ECG device is founded on the Vedic multiplier.

A widely used stick-on temporary electrode is inserted in the subject's (patient's) twin arms to pick up the ECG signal from the body, which can be amplified to 1 V by the ECG preamplifier circuit.

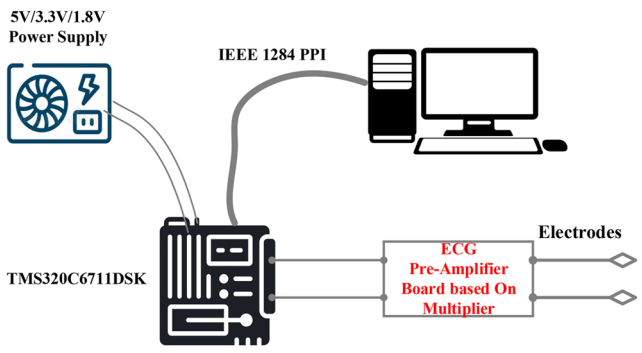

FIG. 4. Block diagram of the ECG signal for DSP starter kit.

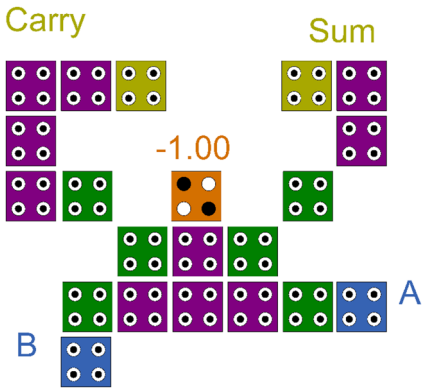

FIG. 5. Proposed half-adder.

The amplifier's output directly connects to the DSK system's codec input.

B. Proposed half-adder

A half-adder is a simple digital gate that performs two-bit binary addition. It involves two inputs (A and B) and two outputs: S (the sum) and C (the carry).[29] Half-adders have an essential function in acting as a basis for computer arithmetic logic. They function at the core of even larger circuits, such as full adders and multi-bit adders, and enable processors to carry out basic operations, such as addition, subtraction, and multiplication.[29] In the lack of such circuits, modern computation and information processing cannot be performed. QCA is a novel nanotechnology that stores binary information in terms of positioning electrons, not a current transistor in traditional technology.[30,31] QCA is accompanied by such advantages as ultra-low power consumption and high device density, outdoing weaknesses in CMOS technology with reduced device dimensions. In QCA, a half-adder is attained through quantum cells that simulate an XOR and an AND function. In most instances, it is a mixture of a majority gate and an inverter optimized for QCA's topology in general. For instance, the XOR gate can be synthesized by combining a majority gate and an inverter. The AND function is a derived function of a one-fixed-input gate of a majority.[30,31] We utilize XOR based on cell interactions[29] to propose a half-adder. Figure 5 shows

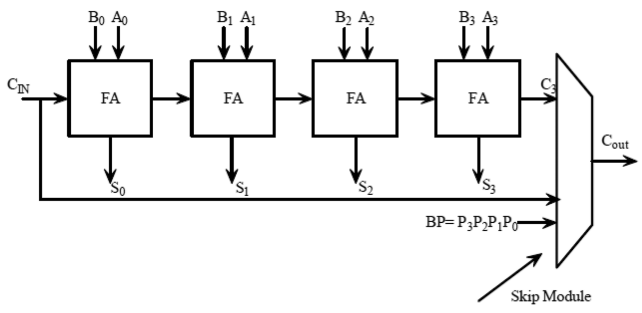

FIG. 6. Four-bit carry skip adder.[32]

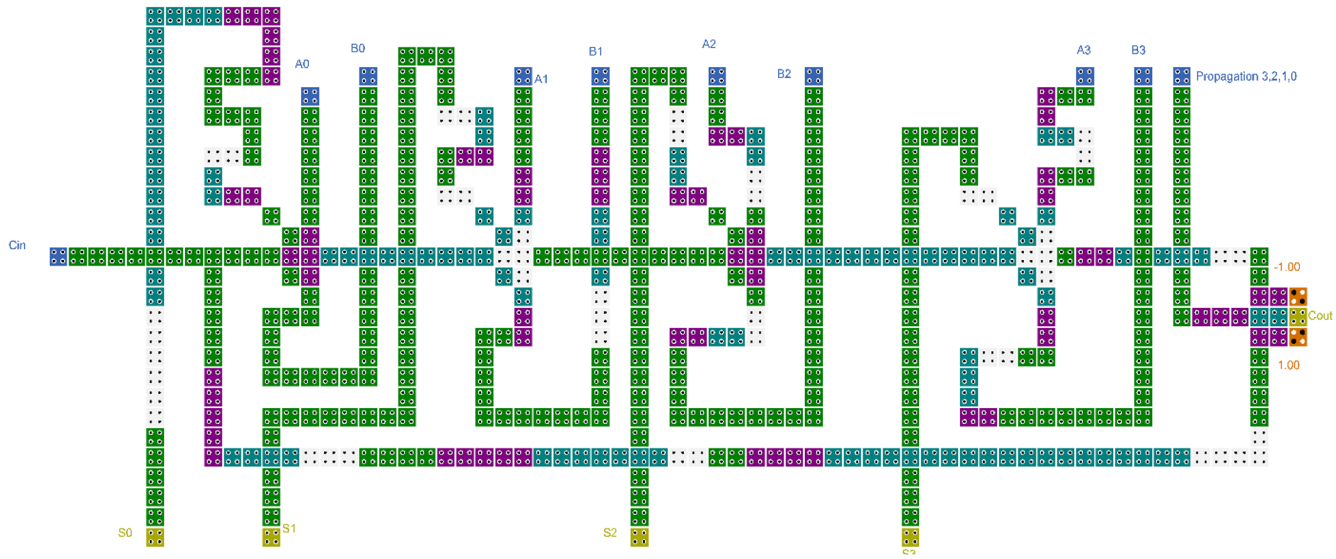

FIG. 7. QCA structure of the proposed CSA.

the proposed QCA half-adder, which comprises one XOR gate with one zero fixed cell, shown in orange. The proposed half-adder is developed through cell interaction. The design consists of 18 cells and provides output after two clock cycles.

This layout makes use of a 0.02 μm^2 area and 21 cells in total. It can also generate accurate results after three clock cycles.

C. Proposed carry skip adder

The carry-skip adder, alternatively referred to as the carry-bypass adder, is a type of adder design that enhances the delay of a ripple-carry adder with a minimal exertion in comparison with alternative adders.[19]

The fundamental concept used here is that carry is moved in an unaltered manner via the bit position for varying A1 and B1 values. In addition, we are utilizing two RCAs for each block, and the number of RCAs can be increased according to our tedious requirements. Its logic comprises AND gates that generate carry and are executed in the second block. The diagrammatic illustration of the carry skip adder circuit is depicted in Fig. 6. The operands utilized here are A and B, both of which have four bits. The first two operand bits are provided to the first RCA, and the next two operand bits are assigned to the second RCA. The carry Cin is set to "0" and assigned to the first RCA. The first RCA's outputs are considered the first two bits of the sum, and the obtained output carry is transferred to the next RCA, which creates the next two bits of the sum. As illustrated

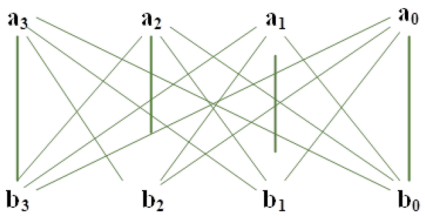

FIG. 8. Urdhva Tiryagbhyam sutra illustration.

b_6	b_5	b_4	b_3	b_2	b_1	a_0	b_4	x	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
								b_0a_7	b_0a_6	b_0a_5	b_0a_4	b_0a_3	b_0a_2	b_0a_1	b_0a_0	
							b_1a_7	b_1a_6	b_1a_5	b_1a_4	b_1a_3	b_1a_2	b_1a_1	b_1a_0	+	
						b_2a_7	b_2a_6	b_2a_5	b_2a_4	b_2a_3	b_2a_2	b_2a_1	b_2a_0	+	+	
					b_3a_7	b_3a_6	b_3a_5	b_3a_4	b_3a_3	b_3a_2	b_3a_1	b_3a_0	+	+	+	
				b_4a_7	b_4a_6	b_4a_5	b_4a_4	b_4a_3	b_4a_2	b_4a_1	b_4a_0	+	+	+	+	
			b_5a_7	b_5a_6	b_5a_5	b_5a_4	b_5a_3	b_5a_2	b_5a_1	b_5a_0	+	+	+	+	+	
		b_6a_7	b_6a_6	b_6a_5	b_6a_4	b_6a_3	b_6a_2	b_6a_1	b_6a_0	+	+	+	+	+	+	
b_7a_7	b_7a_6	b_7a_5	b_7a_4	b_7a_3	b_7a_2	b_7a_1	b_7a_0	+	+	+	+	+	+	+	+	

FIG. 9. Illustration of partial product separation.

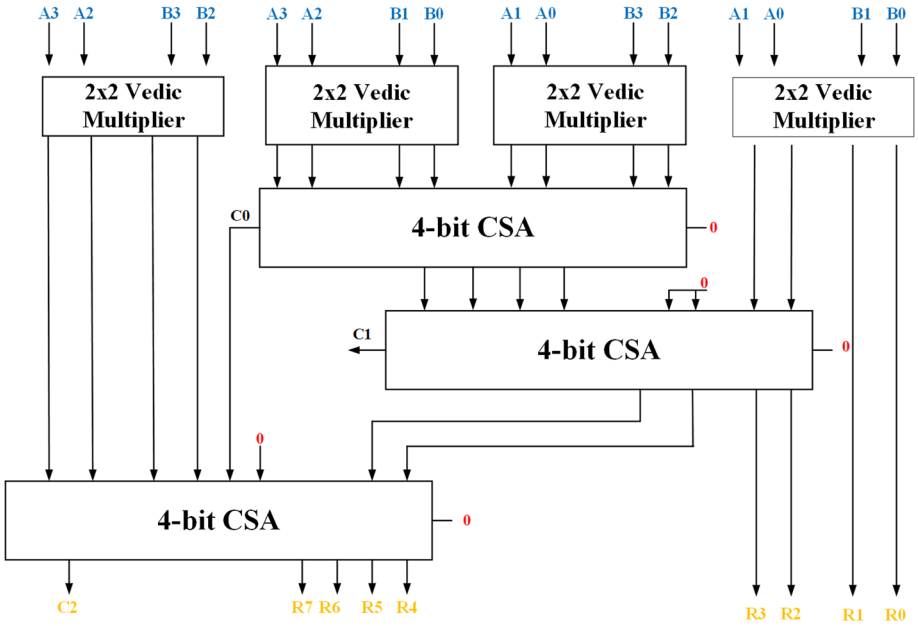

FIG. 10. Block diagram of 4 × 4 Vedic multiplier.[37]

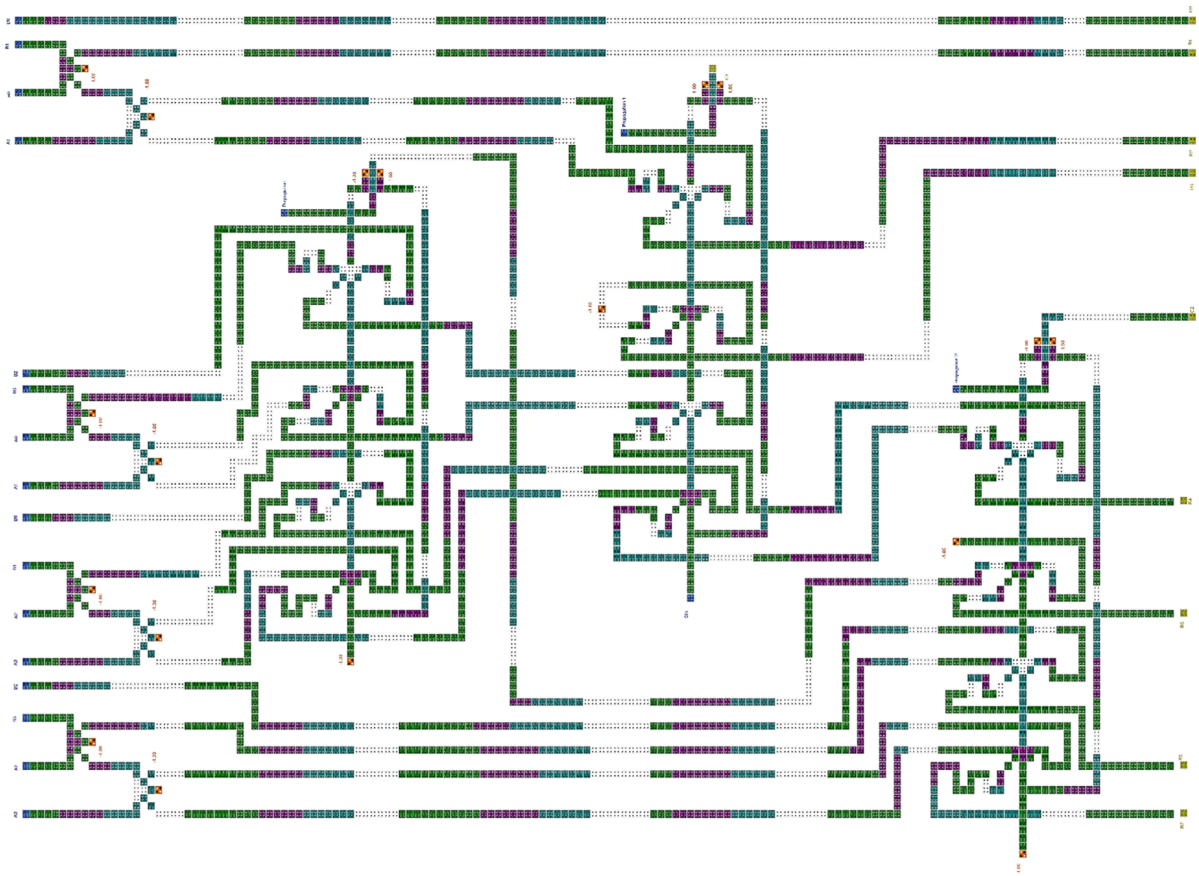

FIG. 11. Structure of the suggested 4 × 4 Vedic multiplier based on CSA.

in Fig. 4, the overall output carry of the circuit includes AND logic and an OR gate.

The CSA is created in QCA using the block layout demonstrated in Fig. 6. Figure 7 illustrates the CSA, which is based on an extraordinary design in Ref. 32. The suggested structure contains one RCA and multiplexer in Ref. 33.

As shown, the suggested CSA is intended to be a low-complexity structure built based on coplanar without rotated cells. This structure employs a total of 325 cells and a 0.70 μm^2 area. It can also generate accurate results after 3.75 clock cycles.

D. Recommended Vedic multiplier

Swami Bharati Krishna Tirthaji Maharaja (1884–1960) rebuilt Vedic mathematics based on Indian scripture known as Vedas.[32] Its foundation is based on 16 principles called word formulas or sutras. Some effective multipliers, such as multiply–accumulate operation, and useful algorithms have been developed in this field, which is quite intriguing. These algorithms are used in engineering, including digital signal processing and computation. Multiplication and Vedic mathematics can be used together to reduce computation time.

Combined multipliers with Vedic mathematics can enhance multiplication operation speed. Urdhva Tiryagbhyam sutra (vertical and cross-wise algorithm) develops the foundation for the multiplier system.[34]

Figure 8 illustrates the Urdhva Tiryagbhyam sutra. It is possible to perform 4 × 4 multiplication using a single line in the Urdhva Tiryagbhyam sutra.[32] However, a conventional technique and four additional partial product shifts are added to acquire effective results.[35]

However, the Urdhva Tiryagbhyam sutra technique requires a few steps to compute the final product in binary multiplication utilization. This, in return, reduces computational time by enhancing the multiplier's speed. In general, the Vedic multiplier requires the methods mentioned below.

Step 1: The outcome of LS is designed by vertically multiplying multiplicand's Least Significant Bit (LSB) with the multiplier.

Step 2: The multiplicand's MSB is multiplied with multiplier's LSB, and the multiplicand's LSB is multiplied with the multiplier's Most Significant Bit (MSB) transversely. Then, the second bit's outcome is generated by adding these products.

Step 3: Multiplicand's MSB and multiplier are multiplied vertically.

The modified Vedic multiplier gate level specifications are shown in Fig. 9. In this design, the Urdhva Tiryagbhyam sutra[32] of Vedic mathematics is combined with the carry by using a carry skip

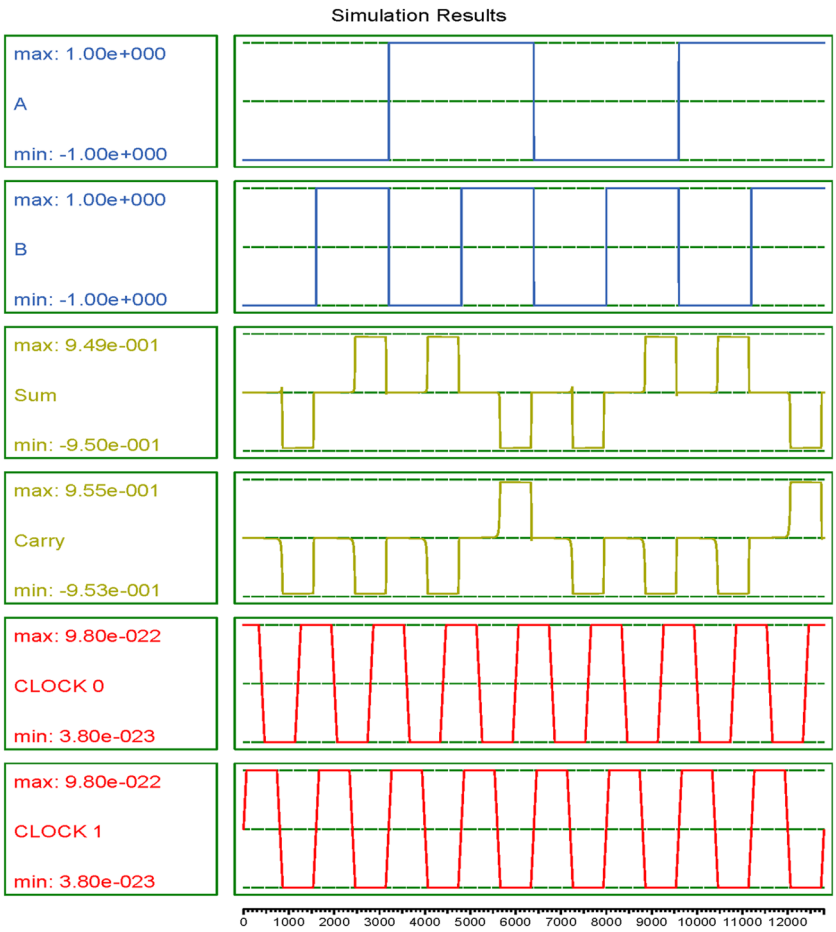

FIG. 12. Simulation results of the half-adder.

method. The computation of each partial product in the multiplication process is explained thoroughly in Fig. 9. If a two-bit carry is generated, a stage is skipped. Speed is elevated by assigning carry to the following stages after the immediate stage. Only half-adders and the carry skip method are used to add input bits.[35]

We also focus on the CSA-based design of a 4 × 4 Vedic multiplier. For explanation, two four-digit integers are considered in this algorithm: A = [$A_3A_2A_1A_0$] and B = [$B_3B_2B_1B_0$]. In step 1, the LSB of number A is multiplied by the LSB of number B to obtain the LSB of the final product. The remaining stages are the same as the process for the 2 × 2 multiplier. The steps of the 4 × 4 Vedic multiplier are realized by a line diagram, as illustrated in Fig. 10, and a CSA adder.[36]

According to the basic notion, the generated carry (Cn) in each step is passed on to the subsequent phase.[37] In addition, the 4 × 4 QCA-based Vedic multiplier is created based on the block design in Fig. 8. As illustrated in Fig. 11, the recommended multiplier structure is designed employing logical and coplanar approaches.

As can be shown, the proposed design is developed in a coplanar structure. This structure uses a total of 3527 cells and a 7.18 μm^2 area. It can also generate accurate output after 4.25 clock cycles.

V. SIMULATION RESULTS

The simulations have been done using a QCADesigner 2.0.3 simulator[35–38] and using the same default options as "bistable approximation,"[38] for instance. Simulation results for the half-adder and the proposed CSA are presented in Figs. 12 and 13. According to the given input, the output vectors in both figures have been generated successfully.

Table II compares the proposed half-adder, CSA, and Vedic multiplier with previous structures based on select evaluation factors: cell count, area occupied, and latency.

It has been demonstrated that the suggested designs outperform the best structures in every parameter. For instance, the recommended half-adder and CSA exhibit a significant improvement

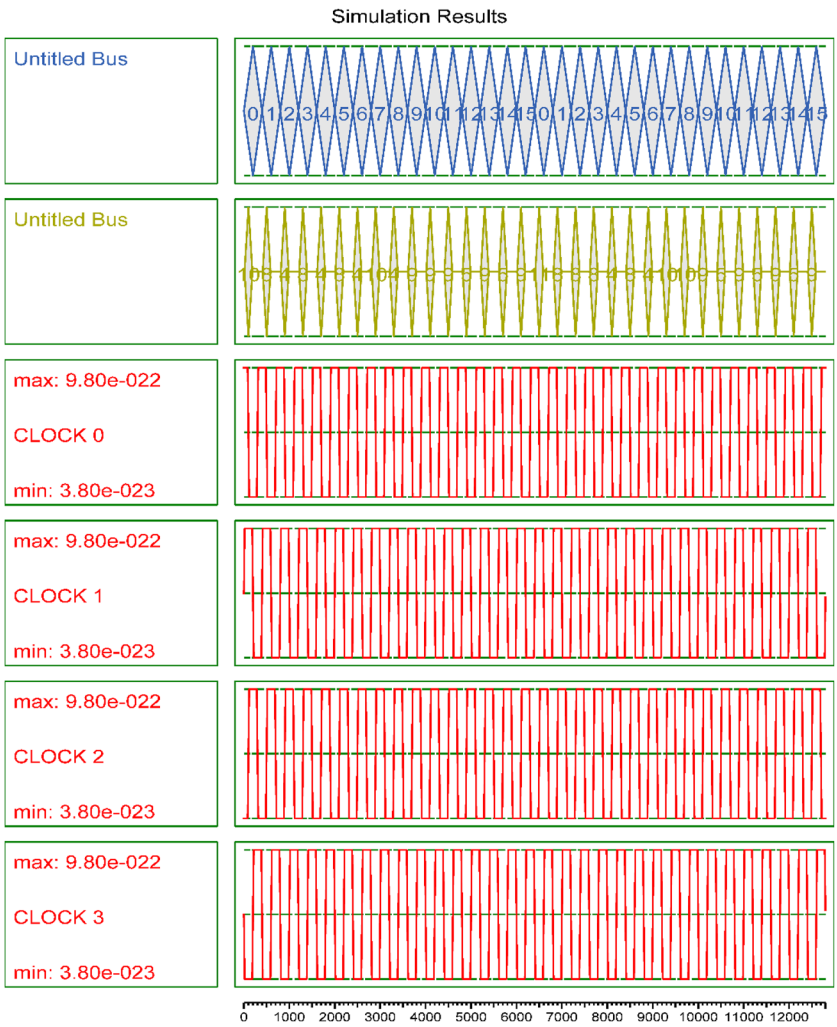

FIG. 13. Results of the simulation for the proposed CSA.

TABLE II. Comparison of HA, CSA, and Vedic multiplier. Boldface denotes the proposed designs.

Design	Cell count	Area (μm^2)	Delay
H-A[39]	77	0.08	1
H-A[40]	61	0.1	0.75
H-A[41]	62	0.08	2
H-A[42]	44	0.05	1
H-A[43]	39	0.04	0.75
Proposed H-A	**21**	**0.02**	**0.5**
Carry skip adder in Ref. 44	1050	2.79	5
Proposed CSA	325	0.70	3.75
Vedic multiplier in Ref. 37	15 673	74.68	66
Vedic multiplier in Ref. 45	13 012	24.80	10
Proposed Vedic	**3527**	**7.18**	**4.25**

in consumed cells and area by 46.15%, 50%, 69.04%, and 74.91%, respectively, in comparison with the current most outstanding structures in Refs. 43 and 44. Furthermore, the suggested Vedic multiplier unit shows a 72.89% enhancement in cell consumption juxtaposed with the multiplier in Ref. 45.

VI. CONCLUSION AND FUTURE WORK

A Vedic multiplier circuit is present in all ECGs, which is crucial to the signal-processing procedure. In order to carry out continuous and complex operations in signal processing programs, the Vedic multiplier circuit always conducts multiplication and accumulation processes. In contrast, the main difficulties in the Vedic multiplier construction are the circuit speed and occupied area. The effectiveness of this key circuit can be significantly increased by fixing these significant flaws. One of the most common ways to overcome all the aforementioned drawbacks, such as speed and dense population areas, is to leverage quantum computing technologies. In other words, a novel quantum technology like QCA technology can readily address all previous drawbacks. Therefore, employing carry skip adder, half-adder, and XOR circuits, this article suggested a quantum multiplier for ECG based on quantum technology. Each of the suggested architectures had a single layer and no rotating cells. Employing the QCADesigner 2.0.3 tool, the recommended architecture was created and verified. The findings demonstrated that all constructed circuits had a straightforward structure with the fewest quantum cells, the best area, and the least latency. Using these research findings as a foundation, the designs can be enhanced with more developed structures to resolve problems in highly complex designs. In addition, evolutionary algorithms can be utilized to investigate the performance of digital filter designs, which is a subject worth more study.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Yuyao Wang: Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Methodology (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Mehdi Darbandi**: Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Methodology (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Seyed-Sajad Ahmadpour**: Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Methodology (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Nima Jafari Navimipour**: Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Methodology (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Ahmad Habibizad Navin**: Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Methodology (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Arash Heidari**: Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Methodology (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Mehdi Hosseinzadeh**: Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Methodology (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Mohammad Anbar**: Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Methodology (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available within the article and from the corresponding authors upon reasonable request.

REFERENCES

[1] A. Varghese, B. Edwards, G. Mitra, and A. P. Rendell, "Programming the adapteva epiphany 64-core network-on-chip coprocessor," Int. J. High Perform. Comput. Appl. **31**(4), 285–302 (2017).
[2] P. Bing, W. Liu, Z. Zhai, J. Li, Z. Guo, Y. Xiang, and L. Zhu, "A novel approach for denoising electrocardiogram signals to detect cardiovascular diseases using an efficient hybrid scheme," Front. Cardiovasc. Med. **11**, 1277123 (2024).
[3] W. Ye, C. Liu, Y. Chen, Y. Liu, C. Liu, and H. Zhou, "Multi-style transfer and fusion of image's regions based on attention mechanism and instance segmentation," Signal Process.: Image Commun. **110**, 116871 (2023).
[4] R. M. Losee, Jr., "Minimizing information overload: The ranking of electronic messages," J. Stud. Int. Educ. **15**(3), 179–189 (1989).
[5] F. Yao, M. S. Zein-Sabatto, G. Shao, M. Bodruzzaman, and M. Malkani, "Nanosensor data processor in quantum-dot cellular automata," J. Nanotechnol. **2014**, 259869.
[6] S. Subathradevi and C. Vennila, "Systolic array multiplier for augmenting data center networks communication link," Clust. Comput. **22**, 13773–13783 (2019).
[7] N. Nagaraju and S. Ramesh, "Implementation of high speed and area efficient MAC unit for industrial applications," Clust. Comput. **22**(S2), 4511–4517 (2019).
[8] M. Goswami, B. Sen, R. Mukherjee, and B. K. Sikdar, "Design of testable adder in quantum-dot cellular automata with fault secure logic," Microelectron. J. **60**, 1–12 (2017).
[9] Y. S. Jeong, J. S. Park, and J. H. Park, "An efficient authentication system of smart device using multi factors in mobile cloud service architecture," Int. J. Commun. Syst. **28**(4), 659–674 (2015).

[10]G. Cocorullo, P. Corsonello, F. Frustaci, and S. Perri, "Design of efficient QCA multiplexers," Int. J. Circuit Theory Appl. **44**(3), 602–615 (2016).
[11]A. N. Oraevsky, "Whispering-gallery waves," Quantum Electron. **32**(5), 377 (2002).
[12]S. Seyedi and N. J. Navimipour, "An optimized design of full adder based on nanoscale quantum-dot cellular automata," Optik **158**, 243–256 (2018).
[13]D. Pan, B.-N. Wu, Y.-L. Sun, and Y.-P. Xu, "A fault-tolerant and energy-efficient design of a network switch based on a quantum-based nano-communication technique," Sustain. Comput.: Inform. Syst. **37**, 100827 (2023).
[14]D. De, T. Purkayastha, and T. Chattopadhyay, "Design of QCA based programmable logic array using decoder," Microelectron. J. **55**, 92–107 (2016).
[15]S. F. Naz, S. Ahmed, S. B. Ko, A. P. Shah, and S. Sharma, "QCA based cost efficient coplanar 1 × 4 RAM design with set/reset ability," Int. J. Numer. Model.: Electron. Netw. Devices Fields **35**(1), e2946 (2022).
[16]M. R. Warnement, I. D. Tomlinson, and S. J. Rosenthal, "Fluorescent imaging applications of quantum dot probes," Curr. Nanosci. **3**(4), 273–284 (2007).
[17]R. Akbari-Hasanjani and R. Sabbaghi-Nadooshan, "New design of binary to ternary converter," IETE J. Res. **69**, 2212–2223 (2021).
[18]F. Ahmad *et al.*, "Performance evaluation of an ultra-high speed adder based on quantum-dot cellular automata," Int. J. Inf. Technol. **11**, 467–478 (2019).
[19]S.-S. Ahmadpour, M. Mosleh, and S. R. Heikalabad, "An efficient fault-tolerant arithmetic logic unit using a novel fault-tolerant 5-input majority gate in quantum-dot cellular automata," Comput. Electr. Eng. **82**, 106548 (2020).
[20]B. K. Mohanty and S. K. Patel, "Area–delay–power efficient carry-select adder," EEE Trans. Circuits Syst. II: Express Br. **61**(6), 418–422 (2014).
[21]S. Verma and V. Sampath Kumar, "Design & analysis of low power, area-efficient carry select adder," Int. J. Eng. Res. Appl. **4**, 53–55 (2012).
[22]G. Savita, V. K. Magraiya, G. Kulshrestha, and V. Goyal, "Designing of low power 16-bit carry select adder with less delay in 45 nm CMOS process technology," Int. J. Emerg. Technol. Adv. Eng. **3**(7), 2250–2459 (2013).
[23]P. Saxena, U. Purohit, and P. Joshi, "Analysis of low power, area-efficient and high speed fast adder," Int. J. Adv. Res. Comput. Commun. Eng. **2**(9), 3705–3710 (2013).
[24]L. Shanigarapu and B. P. Shrivastava, "Low-power and high speed carry select adder," Int. J. Sci. Res. Publ. **3**(8), 1 (2013).
[25]H. Pan, Y. Wang, Z. Li, X. Chu, B. Teng, and H. Gao, "A complete scheme for multi-character classification using EEG signals from speech imagery," IEEE Trans. Biomed. Eng. **71**(8), 2454–2462 (2024).
[26]H. Pan, S. Tong, H. Song, and X. Chu, "A miner mental state evaluation scheme with decision level fusion based on multidomain EEG information," IEEE Trans. Human-Mach. Syst. (published online 2025).
[27]A. Abdelgawad and M. Bayoumi, "High speed and area-efficient multiply accumulate (MAC) unit for digital signal processing applications," in *2007 IEEE International Symposium on Circuits and Systems* (IEEE, 2007), pp. 3199–3202.
[28]J. Shi, L. Bi, X. Xu, A. G. Feleke, and W. Fei, "Low-quality video target detection based on EEG signal using eye movement alignment," Cyborg Bionic Syst. **5**, 0121 (2024).
[29]S.-S. Ahmadpour, M. Mosleh, and S. R. Heikalabad, "A revolution in nano-structure designs by proposing a novel QCA full-adder based on optimized 3-input XOR," Physica B **550**, 383–392 (2018).
[30]S.-S. Ahmadpour, M. Mosleh, and S. Rasouli Heikalabad, "The design and implementation of a robust single-layer QCA ALU using a novel fault-tolerant three-input majority gate," J. Supercomput. **76**(12), 10155–10185 (2020).
[31]H. Cho and E. E. Swartzlander, "Adder designs and analyses for quantum-dot cellular automata," IEEE Trans. Nanotechnol. **6**(3), 374–383 (2007).
[32]J. Swami, S. Bharati Krisna, and T. Maharaja, *Vedic Mathematics or Sixteen Simple Mathematics Formulae from the Veda* (Motilal Banarsidass, Delhi, 1965).
[33]S.-S. Ahmadpour, M. Mosleh, and S. Rasouli Heikalabad, "Efficient designs of quantum-dot cellular automata multiplexer and RAM with physical proof along with power analysis," J. Supercomput. **78**(2), 1672–1695 (2022).
[34]S. R. Huddar, S. R. Rupanagudi, M. Kalpana, and S. Mohan, "Novel high speed Vedic mathematics multiplier using compressors," in *2013 International Mutli-Conference on Automation, Computing, Communication, Control and Compressed Sensing (iMac4s)* (IEEE, 2013), pp. 465–469.
[35]T. Padmavathy, S. Saravanan, and M. Vimalkumar, "Partial product addition in Vedic design-ripple carry adder design fir filter architecture for electro cardiogram (ECG) signal de-noising application," Microprocess. Microsyst. **76**, 103113 (2020).
[36]S. Reshna and M. Jayaraju, "Spotting and recognition of hand gesture for Indian sign language recognition system with skin segmentation and SVM," in *2017 International Conference on Wireless Communications, Signal Processing and Networking (WiSPNET)* (IEEE, 2017), pp. 386–390.
[37]I. Gassoumi, L. Touil, and B. Ouni, "Design of efficient quantum Dot cellular automata (QCA) multiply accumulate (MAC) unit with power dissipation analysis," IET Circuits Devices Syst. **13**(4), 534–543 (2019).
[38]K. Walus, T. J. Dysart, G. A. Jullien, and R. A. Budiman, "QCADesigner: A rapid design and simulation tool for quantum-dot cellular automata," IEEE Trans. Nanotechnol. **3**(1), 26–31 (2004).
[39]S. K. Lakshmi and G. Athisha, "Design and analysis of adders using nanotechnology based quantum dot cellular automata," J. Comput. Sci. **7**(7), 1072 (2011).
[40]H. S. Jagarlamudi, M. Saha, and P. K. Jagarlamudi, "Quantum dot cellular automata based effective design of combinational and sequential logical structures," World Acad. Sci., Eng. Technol. **60**, 671–675 (2011).
[41]P. Z. Ahmad, F. Ahmad, and H. A. Khan, "A new F-shaped XOR gate and its implementations as novel adder circuits based Quantum-dot cellular Automata (QCA)," IOSR J. Comput. Eng. **16**(3), 110–117 (2014).
[42]M. Poorhosseini and A. R. Hejazi, "A fault-tolerant and efficient XOR structure for modular design of complex QCA circuits," J. Circuits Syst. Comput. **27**(07), 1850115 (2018).
[43]N. Safoev and J.-C. Jeon, "Design and evaluation of cell interaction based vedic multiplier using quantum-dot cellular automata," Electronics **9**(6), 1036 (2020).
[44]M. M. Shater and M. R. Faghih, "Design and evaluation of a carry-skip adder in quantum cellular automata technology," J. Electrical Eng. **50**(4), 1673–1682 (2021), https://www.magiran.com/p2244093.
[45]I. Gassoumi, L. Touil, and B. Ouni, "Design of efficient quantum-dot cellular automata (QCA) MAC unit," in *2018 30th International Conference on Microelectronics (ICM)* (IEEE, 2018), pp. 1–4.